UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,311	08/27/2003	Sathya P. Kaginele	M4065.0931/P931	4875

24998 7590 08/11/2006

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
TU, CHRISTINE TRINH LE	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,311	KAGINELE, SATHYA P.	
	Examiner	Art Unit	
	Christine T. Tu	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-14,17,19-23,30,32-36 and 38-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 12-14, 17, 19-23, 30, 32-36 and 38-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. Claims 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8:

At lines 10, the phrase "receiving output signal**s** (**plural**) from said match line**s** (**plural**) ..." cannot be understood. Since only a (**single**) match line is being enabled (as recited at lines 5-6), it is not clear how the (**plurality of**) match line**s** (including the **disabled** match lines) provide output signals. In other words, it is not clear how other disabled match lines) can have any function for providing any output since those match lines **are disabled**.

Claims 9-10:

These claims are rejected because they depend on claim 8 and contain the same problems of indefiniteness.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-7, 8-10, 12-14, 23 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichiriu (7002823) in view of Chadwick et al. (6,430,072 and Chadwick hereinafter).

Claims 1-2:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figures 1 & 5) that, in a CAM device (100), a CAM array (101) includes a plurality of CAM cell arranged in rows for storing CAM words. A comparand register (115) is used to store a comparand value received via the comparand bus (143) and outputs the comparand value to the CAM array (101). During a compare operation, the comparand may be masked by a global mask value, and then compared simultaneously with all the CAM words stored in the CAM array. Each of the rows of CAM cell is coupled to a corresponding match line (182) and any match between the comparand and a valid CAM word results in a match signal being output to the flag circuit (112). The flag circuit (112) then outputs a match flag signal to indicate that a match has occurred (figure 1, column 3 line 29 - column 4 line 34, column 6 lines 42-45).

Ichiriu states that a decoder (103) inside the CAM device (100) decodes a selected address to activate one of a plurality of word lines (181) (column 5 lines 17-23, column 3 lines 54-56).

Ichiriu further states that at the start of a comparison operation, feature of precharging each of the match lines (182) to a high logical level (column 6 line 61-column 7 line 4).

Ichiriu does not explicitly teach the enabling out from the match line under test. Ichiriu, however, teach that unless a host is programmed to read all the locations in the CAM array, it is likely that numerous CAM array locations will not be checked (column 4 lines 26-29).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Ichiriu's CAM array (101) would have been compared partially instead of comparing all the CAM words in the CAM array (101). One having ordinary skill in the art would be motivated to realize so because Ichiriu states that numerous CAM array locations will likely not to be checked (column 4 lines 26-29).

Ichiriu does not explicitly teach the feature of comparing the result of the search operation with an expected result of said search operation, and wherein the expected result comprising an expected match indication on the match line under test. Chadwick however teaches (figures 5, 6 & 8, column 5 line 4-column 6 line 32) that a CAM architecture comprises matchline compare latches/circuit (26) for receiving outputs of the matchlines (15) and then testing the matchlines (column 5 lines 4-47). Chadwick also teaches that the operation of his CAM architecture such that matchlines are tested by performed on a single address sequentially. The test operation includes the steps of (1) loading a data pattern "01010101" in a desired address/word (63), (2) fully discharging every matchline and (3) performing a search operation on the data pattern contained in the word (63) causing a match on this word and a mismatch on the other words. Such match results are testable via the compare shift register and compare circuits (figure 5 [item 26] and figure 6, column 5 line 59-column 6 line 32).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Ichiriu's CAM device (100) would have been comprises Chadwick's compare circuit (26) and perform Chadwick's test operation for testing proper operation of all matchlines. One having ordinary skill in the art would be motivated to realize so because Chadwick teaches that matchlines should be completely tested in order to provide a comprehensive test in CAM designs (column 6 lines 48-59).

Claim 3:

Ichiriu teaches that the CAM array (101) includes circuitry to force validity value with each validity storage cell (202) to a reset state to prevent assertion of a match signal by pulling the match line low for the corresponding row of CAM cells (column 7 lines 49-65, column 8 lines 20-24).

Claims 4-5:

Ichiriu's decoder (105) is a state machine that transitions from state to state in response to transitions of a clock signal (CLK) (104) (column 4 lines 57-67).

Claims 6-7:

Ichiriu teaches that each row of CAM cells (201) is coupled to a respective match line (182) (figure 5, column 6 lines 33-37).

Claims 8-9:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figure 1) that a CAM array (101) includes a plurality of CAM cell arranged in rows for storing CAM words. A comparand register (115) is used to store a comparand value received via the comparand bus (143) and outputs the comparand value to the CAM array (101). During a compare operation, the comparand may be masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array. Each of the rows of CAM cell is coupled to a corresponding match line (182) and any match between the comparand and a valid CAM word results in a match signal being output to the flag circuit (112). The flag circuit (112) then outputs a match flag signal to indicate that a match has occurred (figure 1, column 3 line 29 - column 4 line 34, column 6 lines 42-45).

Ichiriu does not explicitly teach the enabling of the match line of a set of memory cell. Ichiriu, however, teach that unless a host is programmed to read all the locations in the CAM array, it is likely that numerous CAM array locations will not be checked (column 4 lines 26-29).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Ichiriu's CAM array (101) would have been compared partially instead of comparing all the CAM words in the CAM array (101). One having ordinary skill in the art would be motivated to realize so because Ichiriu states that numerous CAM array locations will likely not to be checked (column 4 lines 26-29).

Ichiriu does not explicitly teach the feature of receiving output signals from matchlines and determining such output signals. Chadwick however teaches (figures 5, 6 & 8, column 5 line 4-column 6 line 32) that a CAM architecture comprises matchline compare latches/circuit (26) for receiving outputs of the matchlines (15) and then testing the matchlines (column 5 lines 4-47), figure 5 [item 26] and figure 6, column 5 line 59-column 6 line 32).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Ichiriu's CAM device (100) would have been comprises Chadwick's compare circuit (26) for testing proper operation of all matchlines. One having ordinary skill in the art would be motivated to realize so because Chadwick teaches that matchlines should be completely tested in order to provide a comprehensive test in CAM designs (column 6 lines 48-59).

Claim 10:

Ichiriu teaches that a comparand value is stored to the CAM array (101). Ichiriu also teaches that the results of any match between the comparand and a valid CAM word are outputted to a priority encoder (114) for outputting a CAM index (174), such a CAM index an address of the CAM word corresponding to the selected match signal (column 4 lines 1-8).

Claims 12 and 14:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figures 5 and 1) that a CAM array (101) includes a plurality of CAM cells (201) arranged in rows and columns, with each row of CAM cells (201) being coupled to a respective word line and to a respectively match line (182). Each CAM (201) includes a compare circuit to compare the content of the memory cell with a comparand signal (figure 5, column 6 line 33-column 7 line 13).

Ichiriu does not explicitly teach a circuit for determining a status of the matchline line under test based on a result of a search operation and a signal on the match line under test. Chadwick however teaches (figures 5, 6 & 8, column 5 line 4-column 6 line 32) that, during a search function, a CAM architecture comprises matchline compare latches/circuit (26) for receiving outputs of the matchlines (15) and then testing the matchlines to determining proper operation of each matchlines (column 5 lines 4-47), figure 5 [item 26] and figure 6, column 5 line 59-column 6 line 32).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Ichiriu's CAM device (100) would have been comprises Chadwick's compare circuit (26) for testing proper operation of all matchlines. One having ordinary skill in the art would be motivated to realize so because Chadwick teaches that matchlines should be completely tested in order to provide a comprehensive test in CAM designs (column 6 lines 48-59).

Claim 13:

Ichiriu also teaches a priority encoder (114), in responsive to the results of any match between the comparand and a valid CAM word, for outputting a CAM index (174), such a CAM index an address of the CAM word corresponding to the selected match signal (column 4 lines 1-8).

Claim 23:

This claim is similar to claim 12 with additional processing system having a processor. Ichiriu shows a system (960) including a CAM device (961), a CPU (962) and a network processing unit (NPU) (963) (figure 38, column 37 lines 26-45).

Claim 42:

This claim is similar to claims 1 and 23 with additional processing system having a processor. Ichiriu shows a system (960) including a CAM device (961), a CPU (962) and a network processing unit (NPU) (963) (figure 38, column 37 lines 26-45).

4. Claims 17, 19-22, 30, 32-36 and 28-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichiriu (7,002,823).

Claim 17:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figure 5) that a CAM array (101) includes a plurality of CAM cells (201) arranged in rows and columns, with each row of CAM cells (201) being coupled to a respective word line. Each CAM (201) includes a compare circuit to compare the content of the memory cell with a comparand signal (figure 5, column 6 line 33-column 7 line 13).

Ichiriu does not explicitly teach the enabling circuitry for enabling the match lines. It would have been obvious to one skilled in the art at the time the invention was made to realize that a circuitry being named as "enabling circuitry" would have been included in Ichiriu's CAM device so that every Ichiriu's match line is precharged to a high logical level for a comparison operation. One having ordinary skill in the art would be motivated to realize so because Ichiriu teaches that each of the match lines (182) is precharged to high logical level at the beginning of a comparison operation, but is pulled down to a low logical level by the compare circuit within any attached CAM cell (201) that receives comparand signals which do not match the stored data value (column 6 line 64-column 7 line 4).

Claim 19:

Ichiriu teaches each row of CAM cells (201) is coupled to a respective word line (181) and to a respective match line (182) (figure 5, column 6 lines 35-37).

Claims 20-21:

These claims are similar to claim 17 and 19 with additional recited control circuitry for resets the enabling circuitry. Ichiriu teaches that the CAM array (101) includes circuitry to force validity value with each validity storage cell (202) to a reset state to prevent assertion of a match signal by pulling the match line low for the corresponding row of CAM cells (column 7 lines 49-65, column 8 lines 20-24).

Claim 22:

Ichiriu teaches that a comparand value is stored to the CAM array (101). Ichiriu also teaches that the results of any match between the comparand and a valid CAM word are outputted to a priority encoder (114) for outputting a CAM index (174), such a CAM index an address of the CAM word corresponding to the selected match signal (column 4 lines 1-8).

Claims 30, 32-35:

Claims (30 & 32), (33-35) are rejected for reasons similar to those set forth against claims (17 & 19), (20-22), respectively.

Claims 36 & 38:

These claims are similar to claims 17 & 19 except that a router is being recited. Ichiriu teaches a routing device including a CAM device (961) (figure 38, column 37 lines 26-45).

Claims 39-41:

These claims are similar to claims 20-22 except that a router is being recited. Ichiriu teaches a routing device including a CAM device (961) (figure 38, column 37 lines 26-45).

5. Applicant's arguments with respect to claims 1-7, 8-10, 12-14, 23 and 42 have been considered but are moot in view of the new ground(s) of rejection.

For claims 1, 8, 12, 23 and 42, applicant argues that Ichiriu does not teach the features of testing physical match lines for error. Such feature of testing match lines in a CAM device is now taught by the combination of Ichiriu and Chadwick (see art rejection in paragraph 3 above).

For claims 17, 20, 30, 33, 36 and 39, applicant also argues that Ichiriu does not teach comparison circuitry that determines whether items of data stored in a set of memory cells match a data stored in a comparand register and provides a match signal when a match does occur. Examiner, however, respectfully traverses applicant's remark. Ichiriu does teach such comparison circuitry. Ichiriu teaches that in Fig 5, each CAM cell (201) includes a memory cell to store at least one bit of data, and a compare circuit to compare the content of the memory cell with a comparand signal. Ichiriu also teaches that during a comparison operation, each of the match lines (182) is precharged to a high logic level, but later pulled down to a low logical level by the

compare circuit within any attached CAM cell (201) that receives comparands signals which do not match the stored data value. In other words, any match line (182) not pulled low constitutes a match signal (column 6 lines 42-47, column 6 line 61-column 7 line 4).

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christine T. Tu
Primary Examiner
Art Unit 2138

August 3, 2006